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Fabrication and comparative study of top-gate and bottom-gate ZnO–TFTs with various insulator layers

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Abstract Transparent ZnO thin film transistors (ZnO–TFTs) with different structures and dielectric layers were fabricated by rf magnetron sputtering. The $PbTiO_3$, AlO_x, SiN_x and SiO_x films were attempted to serve as the gate dielectric layers in the devices, respectively, and XRD was employed to investigate the crystal structure of ZnO films deposited on these dielectric layers. The optical properties of transparent TFTs were measured and revealed the average transmittance ranged from 60 to 80% in the visible part of the spectrum. Electrical measurement shows the properties of the ZnO–TFTs have great relations with the device structure. The bottom-gate TFTs have better behaviors than top-gate ones with the mobility, threshold voltage and the current on/off ratio of 18.4 $cm^2 V^{-1} s^{-1}$, -0.7 V and 10^4, respectively. The electrical difference of the devices may be due to different character of the interface between the channel and dielectric layers.

1 Introduction

Thin film transistors (TFTs) have been widely used in flat panel displays in the past decades. The semiconductor channel of TFTs plays an important role in the devices, which can determine the electrical performance and the fabrication process [1–3]. In recent years, thin film transistors with the ZnO channel layer have been investigated extensively due to their potential to replace amorphous (*a*-Si) or polycrystalline silicon (poly-Si) TFTs, which are now used in active matrix displays such as liquid crystal displays and organic light emitting diodes [4–6]. ZnO is a wide band gap compound semiconductor with hexagonal wurtzite structure and has large exciton banding energy, high transparency, excellent chemical and thermal stability. It is one of a few oxides that can be well-oriented grown on various substrates at relatively low temperature [7, 8]. Many methods were used to deposit good quality polycrystalline ZnO films, such as sputtering, pulsed laser deposition, molecular beam epitaxy and chemical solution deposition, etc., and some extra functions such as photodetect and gas-sensor were also achieved based on ZnO–TFTs [9, 10]. However, as far as to now, considerable efforts are under way to improve the field effect mobility, decrease the processing temperature and develop strategies to reduce the carrier density in the channel. There are few reports on the construction ZnO–TFTs with different structures and dielectric layers. In this paper, we report on the fabrication of top-gate and bottom-gate ZnO–TFTs with different dielectric layers. It was found that different structures produce different electrical properties. The ZnO–TFTs with bottom-gate structure have better electrical performance than those with top-gate structure.

2 Experimental details

Figure 1 show the schematic structures of bottom-gate (a) and top-gate (b) ZnO–TFTs. $PbTiO_3$, AlO_x, SiN_x and SiO_x films were attempted to serve as the gate dielectric, respectively. The $PbTiO_3$ film with a thickness of $\sim$250 nm was fabricated by Sol–Gel process [11], the SiN_x film with a thickness of $\sim$250 nm was grown by

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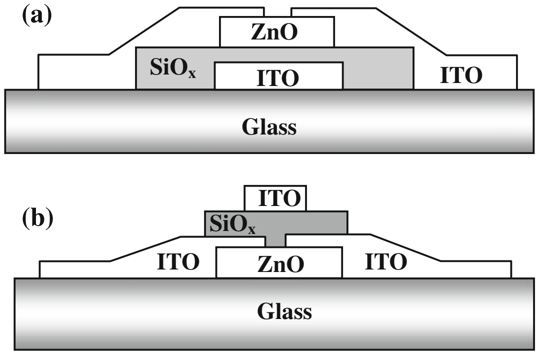

Fig. 1 Schematic cross-sectional illustrations of bottom-gate (**a**) and top-gate (**b**) structure ZnO–TFTs

chemical vapor deposition, the AlO_x and SiO_x films were deposited by rf magnetron sputtering and the thickness was both ~200 nm. The patterns of ZnO film with the area of 800 × 800 μm^2 and the ITO electrode (source and drain) were defined by photolithography techniques. The channel width (W) and length (L) were 100 μm and 20 μm, respectively. The ZnO films were deposited by rf magnetron sputtering at room temperature, using a commercially available ceramic ZnO target (99.99%). The sputtering was carried out in a mixed atmosphere of Ar and O_2 with the flow rate ratio of 3:1. The background pressure was pumped to 6×10^{-4} Pa and the sputtering pressure was maintained at 0.7 Pa. The distance between target and the substrate was 70 mm and the rf power was 100 W. The thickness of ZnO film measured by surface profilometer was 100 nm. Then, the as-deposited ZnO films were submitted to post-thermal annealing at 500 °C in oxygen for 1 h to improve the conductivity. The ITO source and drain were also deposited by rf magnetron sputtering at room temperature and submitted to thermal annealing at 300 °C to form good ohmic contacts with the channel layer.

The crystal structure of ZnO films were investigated by X-ray diffractometry (XRD; DX2000) with CuKα radiation ($\lambda = 0.154184$ nm) in θ–2θ scan mode. The operation voltage and current were 35 kV and 30 mA, respectively. The surface morphology was characterized by atomic force microscopy (Nanoscope IIIa). The optical transmittance of the transparent ZnO–TFTs was performed with a UV–VIS-NIR double beam spectrophotometer (Varian cary 5000) in the wavelength from 300 to 1,200 nm. The electrical characteristics of the ZnO–TFTs were measured by a semiconductor parameter analyser (KEITHLEY 4200).

3 Results and discussion

Figure 2 shows the XRD patterns of ZnO films deposited on $PbTiO_3$, SiO_x, SiN_x and AlO_x dielectric layers, respectively.

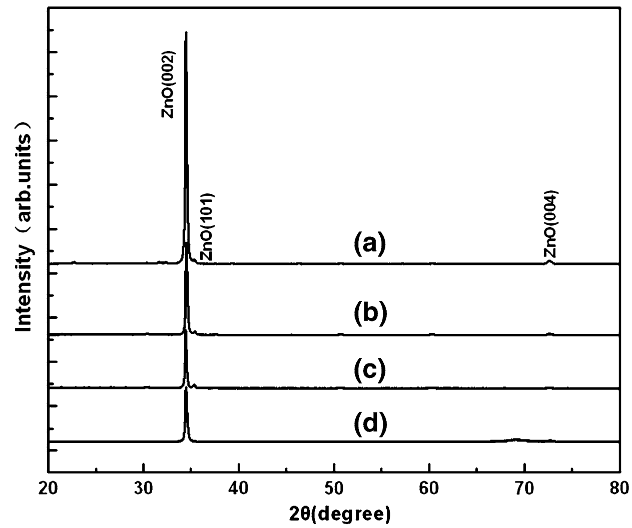

Fig. 2 X-ray diffraction patterns of the ZnO films deposited with different dielectric layers (**a** $PbTiO_3$ **b** SiO_x **c** SiN_x **d** AlO_x)

All the ZnO films show a predominant diffraction peak around 34.4° corresponding to ZnO(002) orientation and a weak ZnO(004) peak, which revealed the films were grown with a preferred c-axis orientation normal to the substrates. Weak ZnO(101) peaks were also observed in the spectra, indicating that the structure of ZnO films has small relation with the dielectric layer. The crystallinity of ZnO films was improved in the order on $PbTiO_3 > SiO_x > SiN_x > AlO_x$ according to the investigated intensities of ZnO(002) peaks [12]. The reason probably is the perovskite structure of $PbTiO_3$ dielectric layer, which leads to higher quality of ZnO film than amorphous layers.

Figure 3 presents the optical transmittance of transparent ZnO–TFTs construct on glass substrates. The absorption edge was all observed at about 382 nm, which is corresponding to the band gap of ZnO films. The structures exhibit oscillations due to interference effects, which demonstrate good interface between all layers. The transistors were highly transparent in the visible light region with the average transmittance of 80% close to the ITO substrates, except that the device with SiN_x dielectric has an average transmittance of about 60%. The reason may be that the radical containing hydrogen in SiN_x causes the reduction of the indium-oxide to metallic indium on the film surface and finally the decrease of transmittance in visible range. However, this phenomenon could be simply avoided by reducing SiH_4 flow rate [13]. The inset of Fig. 3 is the photo of a two inch glass substrate with 44 devices of ZnO–TFT with SiO_x dielectric. Through it the underlying text is visible, which demonstrate the high transparency of the transistors.

The electrical properties of the ZnO films were measured by van der Pauw method in dark at room temperature. The results revealed the as-deposited ZnO film is quite insulating with a resistivity higher than 10^5 Ω cm.

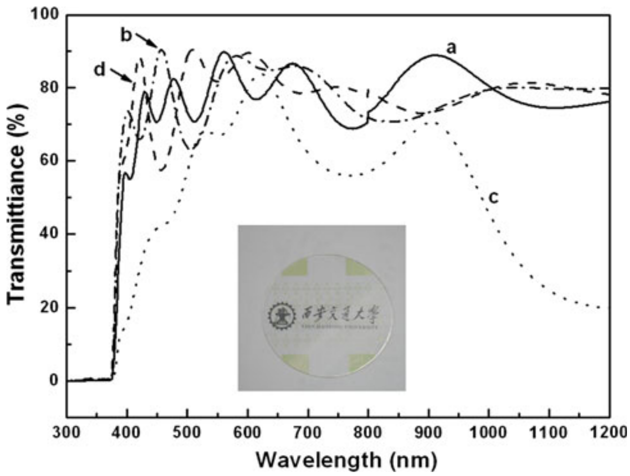

Fig. 3 The optical transmittance of ZnO–TFTs fabricated with different dielectric (**a** $PbTiO_3$ **b** SiO_x **c** SiN_x **d** AlO_x)

The reason may be that the low grown temperature cause high density of the intrinsic defects (Zn interstitials and associated oxygen vacancies) which governed the electrical conductivity of the films. Annealing was used to release some of the defects and improve the electrical properties of the ZnO channel layer [14]. When annealed in oxygen, the electrical resistivity, electron concentration and Hall mobility of the ZnO films were measured to be 46 Ω cm, 1.5×10^{15} cm^{-3} and 89 cm^2 V^{-1} s^{-1}, respectively. It was also found that the electrical properties of ZnO films deposited on dielectric buffer layer mentioned above are similar, even the crystalline properties are different slightly. Figure 4 shows the AFM images of ZnO films deposited on different dielectric layers. The AFM worked in a tapping mode and the scanning area was 1.5×1.5 μm. In light of the images, the films all possessed granular morphology with the grain size ranging from 50 to 120 nm, and the ZnO film deposited on $PbTiO_3$ dielectric has largest grain size consistent with the XRD results.

In this paper, we present the electrical properties of different structure ZnO–TFTs with SiO_x dielectric. Figure 5 shows the output characteristics of bottom-gate structure ZnO–TFTs. The measurements were performed in the dark at room temperature. With the increase of source-to-drain voltage (V_{DS}) at a positive gate bias (V_{GS}), the source-to-drain current (I_{DS}) increases markedly, hence the channel was *n*-type and the electron carriers were generated by the positive V_{GS}.The device operated in enhancement mode because of little drain current at a gate voltage of 0 V. Pinch-off and current saturation are clearly observed, indicating that the entire channel region could be depleted of electrons, which is desirable for most circuit applications.

Figure 6 shows the output characteristics of top-gate ZnO–TFTs. Even though the deposition conditions of the

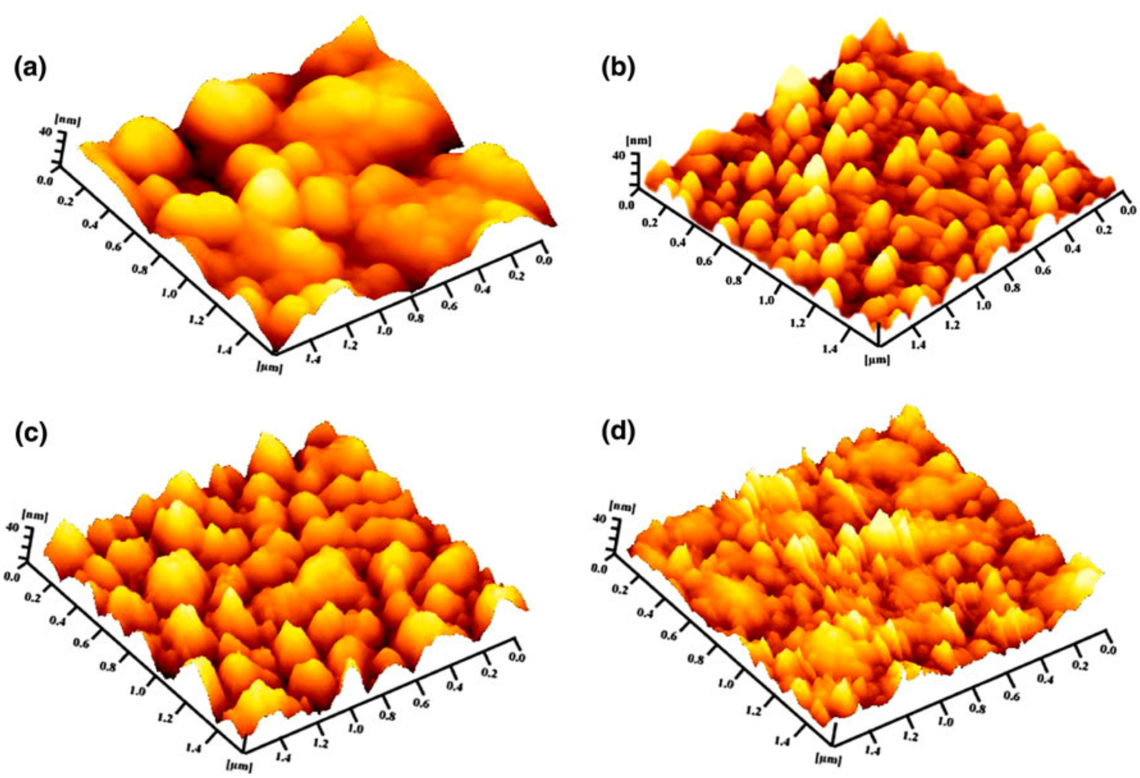

Fig. 4 The AFM image of surface morphology of annealed ZnO film (**a** $PbTiO_3$ **b** SiO_x **c** SiN_x **d**AlO_x)

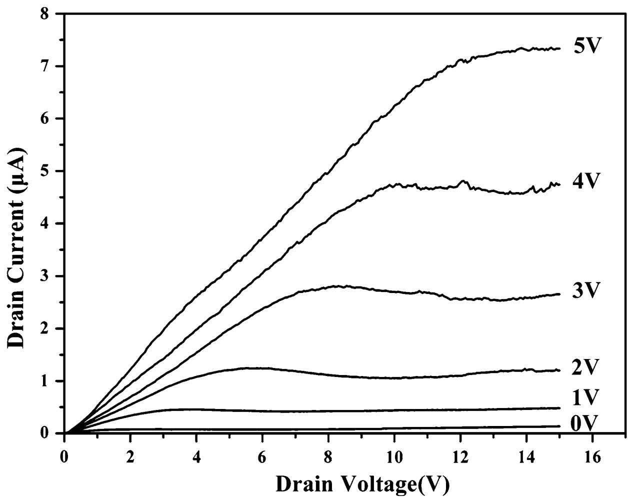

Fig. 5 Output characteristics of the bottom-gate structure ZnO–TFTs

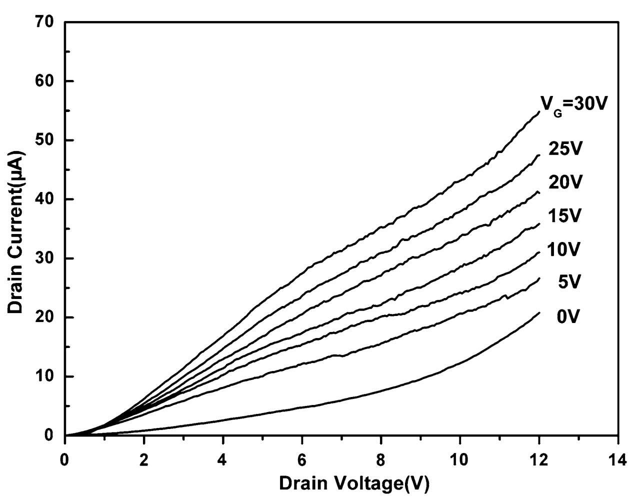

Fig. 6 Output characteristics of the top-gate structure ZnO–TFTs

ITO, ZnO, SiO_x films are the same as those of bottom-gate ZnO–TFTs, the device presents depletion mode performance for there are a large drain current at gate voltage of 0 V and has poorer saturated drain current properties. The channel layer is also *n*-type, but it needs higher gate bias to increase drain current than bottom-gate ZnO–TFTs. The poor electrical performance of the top-gate ZnO–TFTs may due to the degradation of ZnO/SiO_x interface. In our experiment, the sputtering power of SiO_x films was 200 W. The radio frequency induced high energy ions and electrons in the plasma bombard the deposited ZnO layer, which results in the increase of the channel defects. More defects lead to higher carrier concentration which causes the normal-on characteristics of top-gate ZnO–TFTs [15]. Thereby, additional work should be done to optimize the deposition of SiO_x films for good performance top-gate ZnO–TFTs.

The filed effect mobility (μ_{FE}) and the threshold voltage (V_T) can be calculated by the following equation [16] (for the saturation region, $V_{DS} > V_{GS} - V_T$):

$$I_{DS} = \frac{1}{2}\mu_{FE}C_{ox}\frac{W}{L}(V_{GS} - V_T)^2 \tag{1}$$

W and *L* are width and length of the channel, respectively. C_{ox} is the capacitance per unit area of gate dielectric. The transfer curves of the bottom-gate ZnO–TFTs measured at a fixed drain voltage of 8 V were shown in Fig. 7. The V_T was extracted by fitting a straight line to the plot of the square root of I_{DS} versus V_{GS} of -0.7 V. The device exhibited a current on/off ratio of 10^4 and the off current was approximately 3×10^{-10} A. The μ_{FE} was calculated on the order of 18.4 $cm^2\ V^{-1}\ s^{-1}$ according to above mentioned Eq. 1, which is larger one more order of magnitude than that of amorphous silicon TFTs. The channel field effect mobility has great relation to the ratio of *W*/*L*, due to sidewall effects associated with source/drain resistance and to fringing electric field effects that lead to an additional current flow beyond device edges. So, additional work is needed to optimize the *W*/*L* ratio and the device configuration [17].

The subthreshold swing (*S*) defined as the gate voltage required to increase the drain current by a factor of 10 is given by $S = dV_{GS}/d(\log I_{DS})$ [18]. The *S* was estimated on the order of 1 V/decade at the maximum slope in the transfer curve. Besides that, the transistor exhibits a high off-state resistance ($R_{OFF,}$ defined as the inverse of the slope of the *I*–*V* curve for a given gate voltage, in the off saturation regime) larger than 120 MΩ, as required for most circuit applications. The on-state (R_{ON}) defined as:

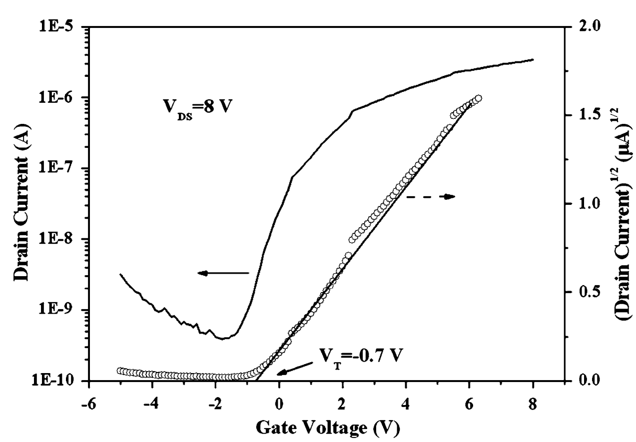

Fig. 7 Transfer characteristics of bottom-gate ZnO–TFTs. The threshold voltage (V_T) was extracted by fitting the linear portion of the $(I_{DS})^{1/2}$ versus V_{GS} curve

$$R_{ON} = \frac{L}{\mu_{FE} C_{ox} W (V_{GS} - V_T)} \quad (2)$$

is of about $R_{ON} = 1.5\ M\Omega$ ($V_{GS} = 5$ V). The ratio of R_{OFF} to R_{ON} is within what is expected for fast switching device behaviors [19, 20].

4 Conclusion

Transparent ZnO thin film transistors with different structures and dielectric layers were fabricated by rf magnetron sputtering. The crystal structure and optical transmittance of ZnO films deposited on different dielectric were investigated by XRD and spectrophotometer. Electrical measurement revealed that the bottom-gate ZnO–TFTs with SiO_x dielectric have better behaviors than top-gate ones. The bottom-gate transistors operate as an *n*-channel enhancement mode having clear pinch off and saturation characteristics. The field effect mobility, threshold voltage and the current on/off ratio were determined of 18.4 $cm^2\ V^{-1}\ s^{-1}$, -0.7 V and 10^4, respectively. The results indicate ZnO films can be used as channel layer of transparent thin film transistor and will play the important role in the future transparent electronic circuits.

References

1. S. Wagner, H. Gleskova, I.C. Cheng, M. Wu, Thin Solid Films **430**, 15 (2003)
2. N. Kenji, O. Hiromichi, U. Kazushige, K. Toshio, H. Masahiro, H. Hideo, Microelectron. Eng. **72**, 294 (2004)
3. F.D. Angelis, T. Toccoli, A. Pallaoro, N. Coppede, L. Mariucci, G. Fortunato, S. Iannotta, Synthetic. Met. **146**, 291 (2004)
4. R. Navamathavan, E.J. Yang, J.H. Lim, D.K. Hwang, J.Y. Oh, J.H. Yang, J.H. Jang, S.J. Park, J. Electrochem. Soc. **153**, 5–G385 (2006)
5. K.T. Kang, M.H. Lim, H.G. Kim II, D. Kim, J.M. Hong, Appl. Phys. Lett. **90**, 043502 (2007)
6. K. Lee, J.H. Kim, S. Lm, C.S. Kim, H.K. Baik, Appl. Phys. Lett. **89**, 13357 (2006)
7. A. Sasaki, W. Hara, A. Matsuda, N. Tateda, S. Otaka, S. Akiba, K. Saito, T. Yodo, M. Yoshimoto, Appl. Phys. Lett. **86**, 231911 (2005)
8. V. Vaithianathan, B.T. Lee, S.S. Kim, J. Appl. Phys. **98**, 043519 (2005)
9. H.S. Bae, S. Im, Thin Solid Films **469–470**, 75 (2004)
10. S. Kandasamy, W. Wlodarski, A. Holland, S. Nakagomi, Y. Kokubun, Appl. Phys. Lett. **90**, 064103 (2007)
11. D. Bao, X. Yao, K. Shinozaki et al., J. Phys. D. Appl. Phys. **36**, 2141–2145 (2003)
12. T. Matsuda, M. Furuta, T. Hiramatsu, C. Li, H. Furuta, H. Hokari, T. Hirao, J. Cryst. Growth **310**, 31 (2008)
13. K.S. Son, D.L. Choi, H.N. Lee, W.G. Lee, Curr. Appl. Phys. **2**, 229 (2002)
14. O. Vigil, F. Cruz, G. Santana, L. Vaillant, A.M. Acevedo, G.C. Puente, Appl. Surf. Sci. **161**, 27 (2000)
15. S. Masuda, K. Kitamura, Y. Okumura et al., J. Appl. Phys. **93**, 1624 (2003)
16. B. Yaglioglu, H.Y. Yeom, R. Beresford et al., Appl. Phys. Lett. **89**, 062103 (2006)
17. E.M.C. Fortunato, P.M.C. Barquinha, A. Pimentel et al., Appl. Phys. Lett. **85**, 2541 (2004)
18. R. Martins, P. Barquinha, I. Ferreira et al., J. Appl. Phys. **101**, 044505 (2007)
19. A.J. Snell, K.D. Mackenzie, W.E. Spear et al., Appl. Phys. **24**, 357 (1981)
20. E. Fortunato, P. Barquinha, A. Pimentel et al., Thin Solid Films **487**, 205 (2005)